TCAD Simulation of Diamond Static Induction Transistors for Radio Frequency Power Amplifiers

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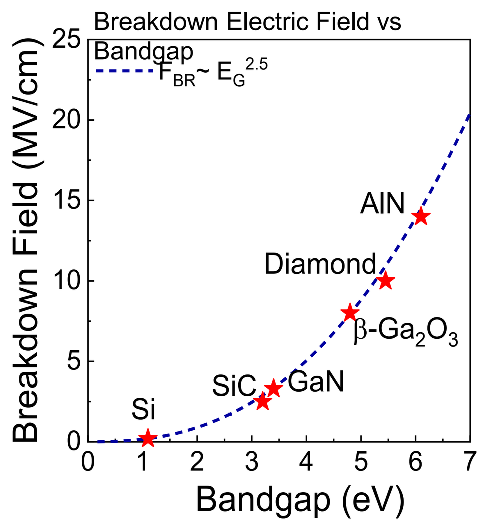
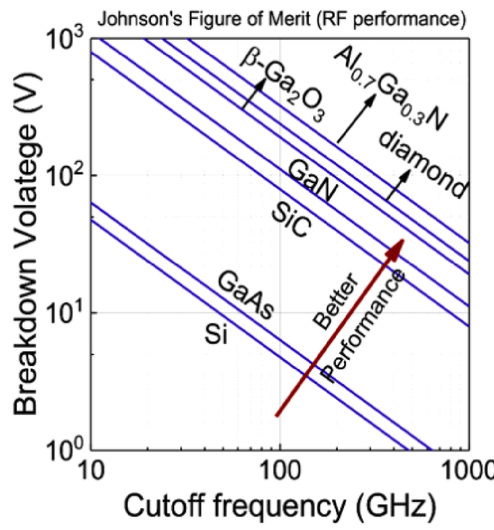
Ultra-wide Bandgap (UWBG) semiconductors for RF Devices

RF/mm-wave applications

Power





- Johnson's figure of merit (FOM) for RF devices, $\boldsymbol{V_{BR} \times f_T = F_{BR} \times v_{sat}/2\pi}$.
- UWBG semiconductors offer high breakdown fields (F_{BR}) and saturation velocity (v_{sat}).
- Enables achieving high power density (P_{out}), gain (G_P) and power added efficiency (PAE).

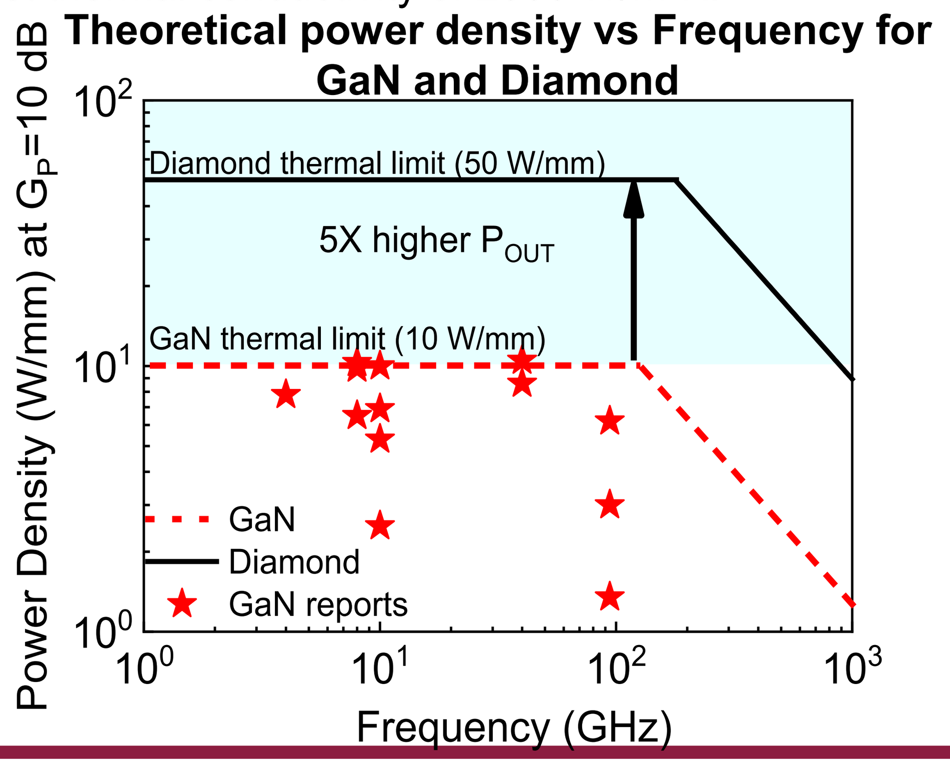
High Power Density Diamond FETs

- Power density of GaN HEMTs on SiC (state of the art RF transistor) is limited to 10 W/mm due to thermal conductivity of SiC substrate (~400 W/m-K).
- **Power density of RF transistors can be increased by 5X** by moving to diamond which has the highest thermal conductivity of 2000 W/m-K.

Theoretical power density of an RF transistor

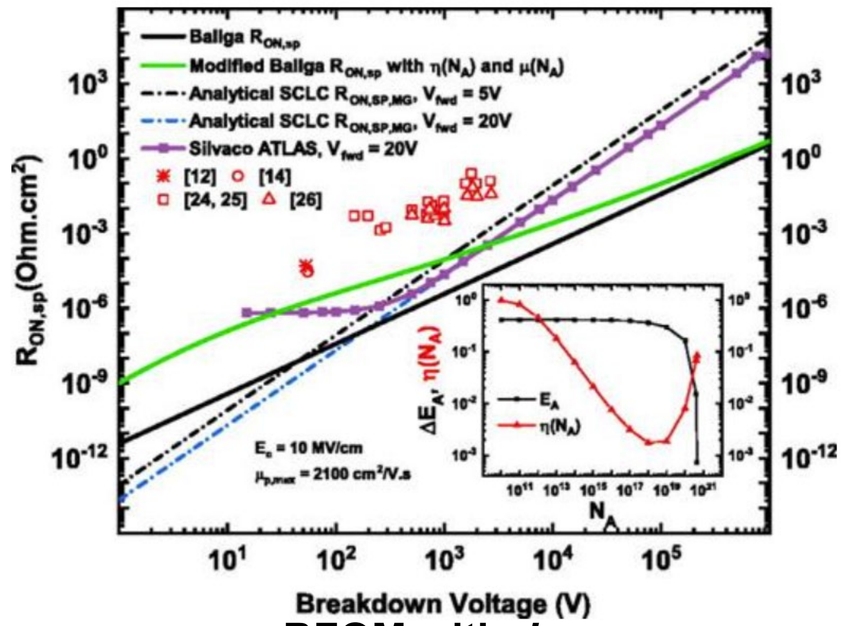
$$P_{out} = \frac{\epsilon F_{BR}^2 v_{sat}^2}{64\pi} \frac{1}{\sqrt{G_p f}} \sqrt{\frac{R_{out}}{R_{in}}}$$

Theoretical power density vs Frequency for GaN and Diamond



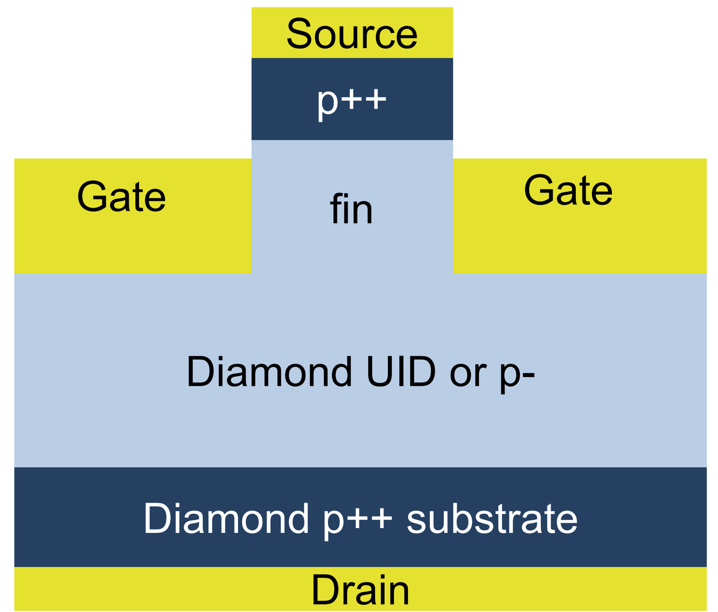
Diamond Static Induction Transistor

- Key limitation in diamond → **Deep donors and acceptors**→ Boron (E_A=0.37 eV), Phosphorus (E_D~0.6 eV).
- Deep donor/acceptor levels limit current density in diamond transistors.
- To overcome this limitation, we study **Static Induction Transistors (SITs)** which enable space charge limited conduction ($\boldsymbol{J_{SCLC}} = \frac{9}{8}\frac{\epsilon\mu V^2}{L^3}$) by injecting carriers from the source contact.
- Space charge limited conduction is effective in diamond for breakdown voltages of ~100 V



BFOM with J_{SCLC}

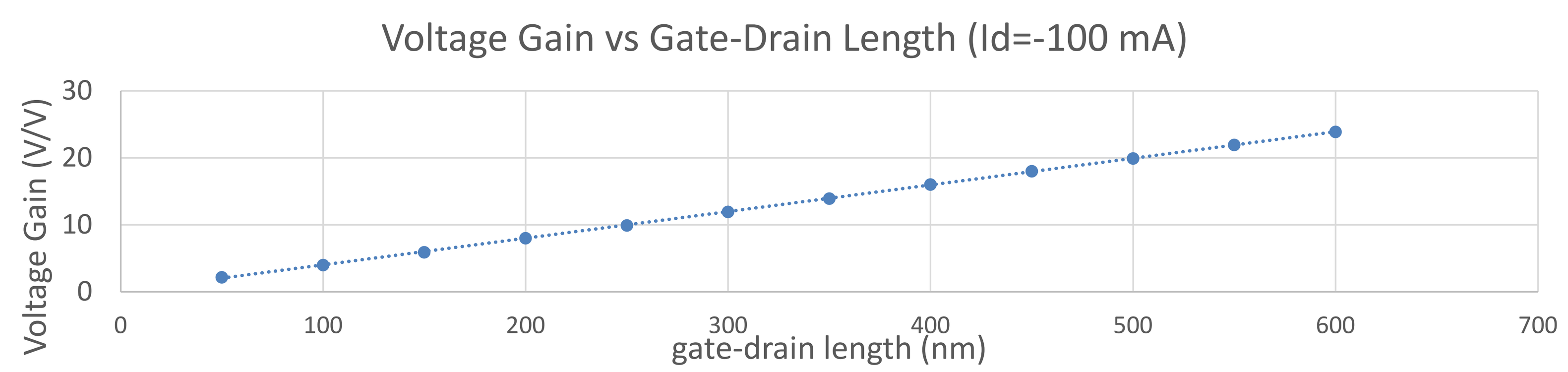
Kok Wai Lee, Yee Sin Ang, *Appl. Phys. Lett.* 2 October 2023; 123 (14)

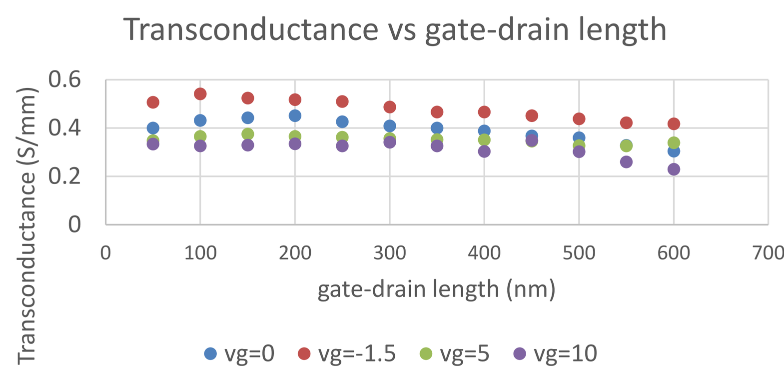


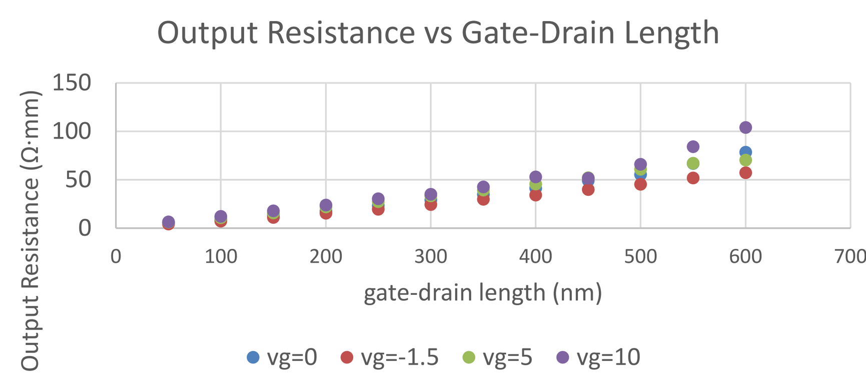
Schematic of diamond SIT

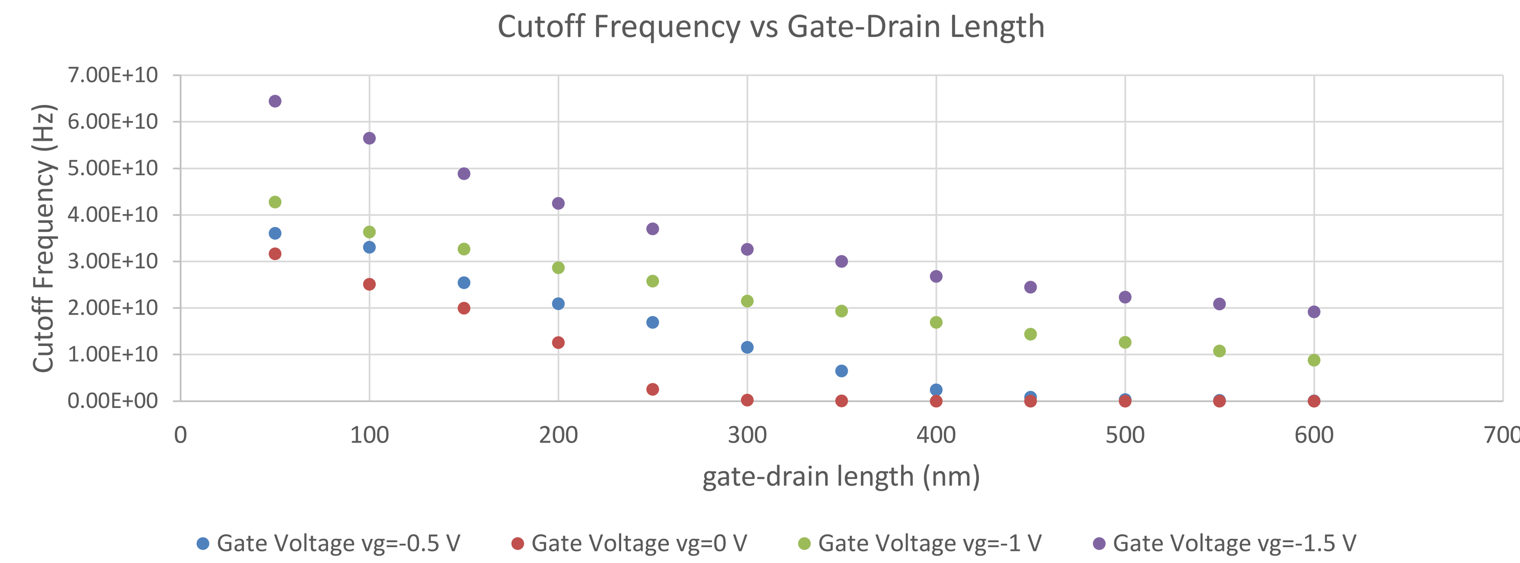
Gate-Drain Length Simulations

- The gate-drain length is a significant device design parameter for RF vertical devices.
- To investigate the design space, RF and I-V simulations were performed using gate-drain lengths in the range of 50-500 nm, drain voltage of -10 V, and varying gate voltages.

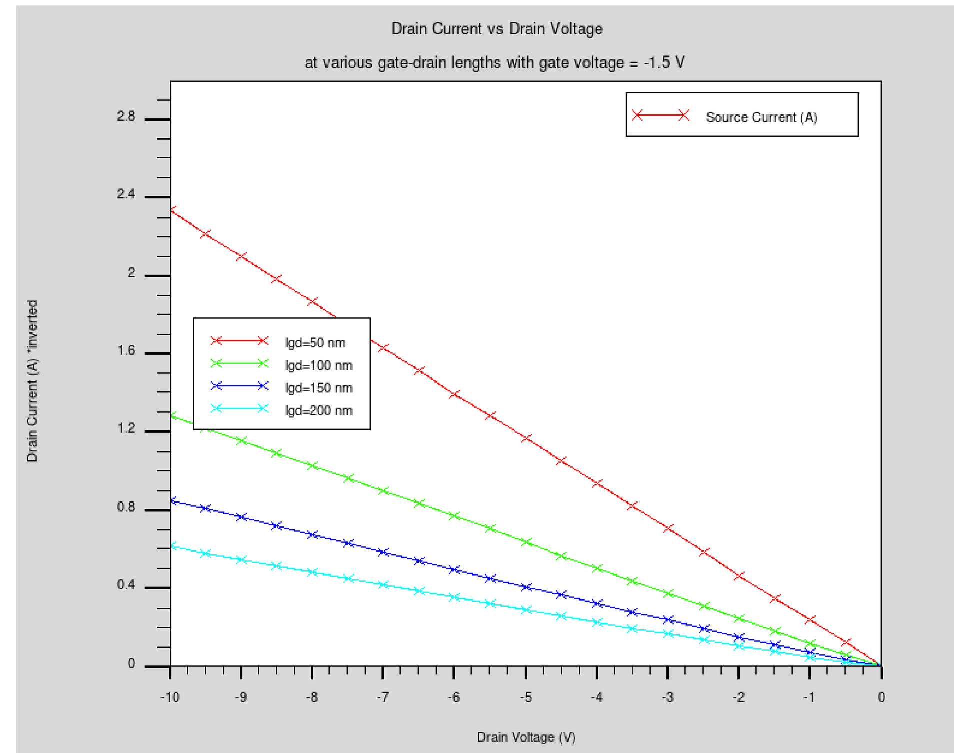








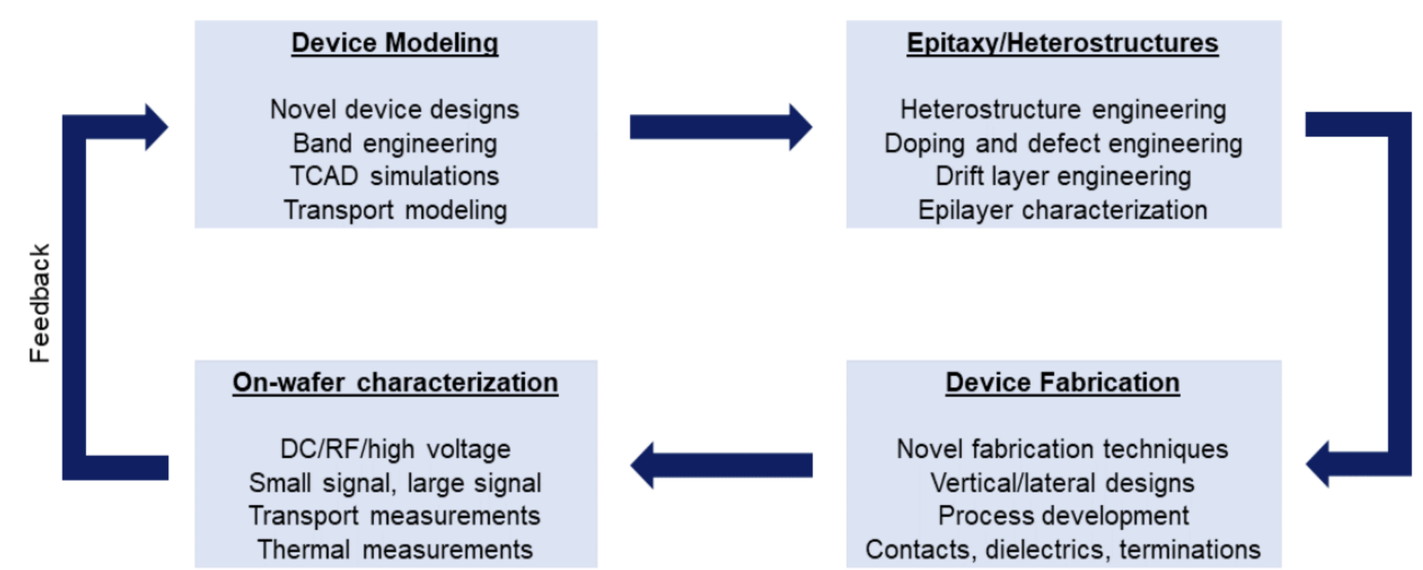
- The gate-drain length dependent behavior of voltage gain, output resistance, and transconductance can be extracted from the I-V simulation.
- The cutoff frequency (f_t) is a vital specification for the design of RF devices.
- The gate-drain length range of 50-200 nm achieved the highest cutoff frequencies and current densities.



Conclusion

- The 50-200 nm gate-drain length range shows the most promise for practical design.
- The next step for this project is to continue the parameter sweep with the aspect ratio (gate length, fin width), source-gate length, and doping profile.
- This project fits completely within the device modeling step of the development process. After simulations are complete, the remaining steps are process optimization, fabrication, and characterization.

Vertically Integrated Semiconductor Device Development



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